AMENDMENT TO CLAIMS

Please amend the claims as follows:

1-22. (Cancelled)

23. (New) A semiconductor device, comprising:

a substrate, and

a semiconductor region formed in a predetermined area of the substrate, said semiconductor region having a predetermined concentration of an impurity and a principal surface, wherein:

in the semiconductor device, a first transistor having a semiconductor FIN structure and a second transistor having a planar structure are integrated in the semiconductor region,

the first transistor includes:

a trench region formed in the semiconductor region so as to have a concave shape with a bottom surface located at a lower position than the principal surface of the semiconductor region, said trench region having first side surfaces,

source/drain regions each of which is formed so as to be buried in the trench region, said source/drain regions containing an impurity,

a semiconductor FIN structure formed in the trench region so as to be buried in the trench region, and located between the source/drain regions, said semiconductor FIN having a convex shape with an upper surface and second side surfaces,

an isolation insulating film formed in the trench region so as to be buried between the source/drain regions and the first side surfaces of the trench region, and between the semiconductor FIN structure and the first side surfaces of the trench region,

a gate insulating film disposed on the upper surface and both side surfaces of the semiconductor FIN structure, and,

a gate electrode disposed on the second side surfaces and the upper surface of the semiconductor FIN structure with the gate insulating film interposed therebetween, and between the second side surfaces of the semiconductor FIN structure and the isolation insulating film,

the second transistor is formed on a part of the principal surface of the semiconductor region outside said trench region, and

the upper surface of the FIN structure of the first transistor does not protrude from the principal surface of the semiconductor region.

24. (New) The semiconductor device of claim 23, wherein an upper surface of each of the source/drain regions of the first transistor and an upper surface of each of the source/drain regions of the second transistor are located substantially at the same level.

25. (New) The semiconductor device of claim 24, wherein the upper surface of the semiconductor FIN structure of the first transistor is located substantially at the same level as those of the upper surfaces of the source/drain regions of the first and second transistors.

26. (New) A semiconductor device comprising:

a substrate, and

a semiconductor region formed in a predetermined area of the substrate, said semiconductor region having a predetermined concentration of an impurity and a principal surface, wherein:

in the semiconductor device, a first transistor having a semiconductor FIN structure and a second transistor having a planar structure are integrated in the semiconductor region,

the first transistor includes:

a trench region formed in the semiconductor region so as to have a concave shape with a bottom surface located at a lower position than the principal surface of the semiconductor region, said trench region having first side surfaces,

source/drain regions each of which is formed so as to be buried in the trench region, said source/drain regions containing an impurity,

a semiconductor FIN structure formed in the trench region so as to be buried in the trench region, and located between the source/drain regions, said semiconductor FIN having a convex shape with an upper surface and second side surfaces,

an isolation insulating film formed in the trench region so as to be buried between the source/drain regions and the first side surfaces of the trench region, and between the semiconductor FIN structure and the first side surfaces of the trench region,

a gate insulating film disposed on the upper surface and both side surfaces of the semiconductor FIN structure, and,

a gate electrode disposed on the second side surfaces and the upper surface of the semiconductor FIN structure with the gate insulating film interposed therebetween, and between the second side surfaces of the semiconductor FIN structure and the isolation insulating film,

the second transistor is formed on a part of the principal surface of the semiconductor region outside said trench region, and

the upper surface of the FIN structure, the principal surface of the semiconductor region, an upper surface of each of the source/drain regions of the first transistor and an upper surface of

each of the source/drain regions of the second transistor are located substantially at the same level.

27. (New) The semiconductor device of claim 23, wherein:

the gate electrode formed on the upper surface of the semiconductor FIN structure of the first transistor extends orthogonally to the direction of a line connecting the source/drain regions of the first transistor, and

the gate electrode extends onto a part of the semiconductor region extending outwardly from the trench region.

28. (New) The semiconductor device of claim 23, wherein the gate electrode of the first transistor has an extension portion extending onto the part of the semiconductor region extending outwardly from the trench region, and an insulation film is formed between the extension portion and the semiconductor region.

29. (New) The semiconductor device of claim 23, wherein a direction in which the gate electrode formed on the upper surface of the semiconductor FIN structure of the first transistor extends is parallel to a direction in which the gate electrode of the second transistor extends.

30. (New) The semiconductor device of claim 23, wherein the gate electrode of the first transistor is formed so that a part of the gate electrode located on the upper surface of the

semiconductor FIN structure has a larger thickness than that of a part of the gate electrode located on each of the side surfaces of the semiconductor FIN structure.

31. (New) The semiconductor device of claim 23, wherein a part of the gate electrode of the first transistor located on each of the side surfaces of the semiconductor FIN structure is made of a first material and a part of the gate electrode located on the upper surface of the semiconductor FIN structure is made of the first material and a second material.

32. (New) The semiconductor device of claim 31, wherein the first material is polysilicon and the second material is silicide.

33. (New) The semiconductor device of claim 23, wherein the gate insulating film is formed so that a part of the gate insulating film located on the upper surface of the semiconductor FIN structure has a larger thickness than that of a part of the gate insulating film located on each of the side surfaces of the semiconductor FIN structure.

34. (New) The semiconductor device of claim 23, wherein the semiconductor FIN structure is made of SiGe or SiGeC.

35. (New) The semiconductor device of claim 23, wherein each of the source/drain regions of the second transistor has a larger width than that of the semiconductor FIN structure.

36. (New) The semiconductor device of claim 23, wherein the semiconductor FIN structure of the first transistor and the source/drain regions of the first transistor form an H shape when viewed from the top.

37. (New) The semiconductor device of claim 23, wherein an LDD region is formed in each of the source/drain regions of the first transistor.

38. (New) The semiconductor device of claim 23, wherein each of the source/drain regions of the first transistor is formed so as to extend from the upper surface of the semiconductor FIN structure to a bottom surface of the semiconductor FIN structure.

39. (New) The semiconductor device of claim 23, wherein the bottom part of the trench region of the first transistor includes a heavily doped impurity layer region having a higher concentration of an impurity than that of the semiconductor region.

40. (New) The semiconductor device of claim 23, wherein the gate electrode formed on the semiconductor FIN structure of the first transistor and the gate electrode of the second transistor are made of the same material.

41. (New) The semiconductor device of claim 23, wherein:

source/drain electrodes are formed respectively on the source/drain regions of the first transistor,

source/drain electrodes are formed respectively on the source/drain regions of the second transistor, and

the source/drain electrodes are made of the same material.

42. (New) The semiconductor device of claim 23, wherein an isolation insulating film is formed between each of the source/drain regions of the second transistors and the semiconductor region.